Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 2, 4, 5, 6, 7 and 9 as described in the attached annotated sheets.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

This application has been carefully reviewed in light of the Office Action dated May 15, 2006. Claims 1-18 remain in this application. Claims 1 and 2 are the independent Claims. Claims 1 and 2 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Applicant thanks the Examiner for granting the September 7, 2006 telephone interview. Reconsideration and entrance of the amendment in the application are respectfully requested.

Objection to the Specification

The present disclosure is objected because of informalities.

Applicant respectfully submits that reference numeral 48 is recited on page 16, line 8 of the present specification. Reference numeral 54 is recited on page 16, line 1 of the specification. The remaining objected to reference numerals have been removed from Figs. 2, 4, 5, 6, 7 and 9.

Reconsideration and withdrawal of the above objections are respectfully requested.

Art-Based Rejections

Claims 1-2 and 13-14 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,655,096 (Branigin); Claims 3-12 and 15-18 stand rejected under §103(a) over Branigin in view of U.S. Patent No. 5,784,584 (Moore). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Branigin Reference

Branigin is directed to a computer processor that employs parallelism through pipelining by Sequential Coherency Instruction Scheduling and/or Sequential Coherency Exception Handling. *(See Branigin, Col. 15, lines 44-64).*

The Moore Reference

Moore is directed to a microprocessor that is directly connected to DRAMs and a microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times. (*See Moore, Col. 1, line 59 to Col. 2, line 2*).

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device using pipeline control.

As defined by amended independent Claim 1, a data processing device using pipeline control includes an instruction queue in which a plurality of instruction codes are fetched, a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue, and a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue. A branch information setting circuit decodes a branch setting instruction, the branch setting instruction explicitly or implicitly specifies a branch address and a branch target address, when the fetch address is the branch address after x-th instruction from the branch setting instruction. The branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded. The fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch

address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "*a branch information setting circuit which decodes a branch setting instruction, wherein the branch setting instruction explicitly or implicitly specifies a branch address and a branch target address, when the fetch address is the branch address after x-th instruction from the branch setting instruction, the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded*", as required by amended independent Claim 1.

Branigin discloses a BRANCH AND LINK instruction, BAND, which when decoded calculates/specifies only a single branch address to which a program is going to branch to when this instruction is encountered. This single branch address is then stored in a register, PC_TOP. (*See, Branigin, col. 62, lines 54-55; col. 65, lines 8-21; col. 88, lines 26-50*)

In contrast, the branch setting instruction of the present invention specifies not only a branch target address, which is indicative of where the program is going to branch to, but also a branch address. The branch address is indicative of the address at which the program is going to branch (jump) to the branch target address. When a branch information setting circuit decodes the branch setting instruction both the branch address and the branch target address are stored in registers. (*See, Specification, pg. 7, lines 1-25*)

Accordingly, Branigin fails to teach or suggest both a "*branch setting instruction explicitly or implicitly specifies a branch address and a branch target address,*" and storing "*the branch address in a branch address storage register and the branch target address in a branch target address storage register*", as required by amended independent Claim 1.

The ancillary Moore reference does not remedy the deficiencies of Branigin.

Since the applied references do not disclose or suggest the above features of the present invention as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

Amended independent Claim 2 is allowable for at least the same reasons as discussed above with reference to amended independent Claim 1 and such allowance is respectfully requested.

The remaining Claims 3-18 depend either directly or indirectly from amended independent Claims 1-2 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the remaining Claims 2-18 are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

Applicant believes the foregoing amendments comply with requirements of form and thus may be admitted under 37 C.F.R. § 1.116(b). Alternatively, if these amendments are deemed to touch the merits, admission is requested under 37 C.F.R. § 1.116(c). In this connection, these amendments were not earlier

presented because they are in response to the matters pointed out for the first time in the Final Office Action.

Lastly, admission is requested under 37 C.F.R. § 1.116(b) as presenting rejected claims in better form for consideration on appeal.

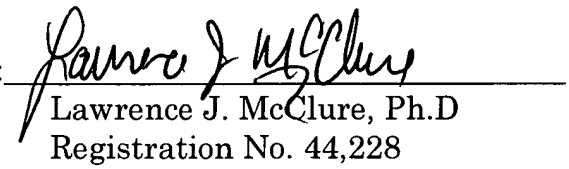
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: September 15, 2006

By: 
Lawrence J. McClure, Ph.D
Registration No. 44,228
for Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701